In the Claims:

Please amend the claims as indicated:

1. (Currently Amended) A method for fabricating sidewall spacers in the manufacture of an integrated circuit device, comprising ~~the steps of~~:

providing a substrate having a gate structure formed thereon;

forming a dielectric spacer layer over the semiconductor substrate; and

etching said dielectric spacer layer without the use of a sacrificial forming spacer~~, prior to forming a layer subsequent to the dielectric layer,~~ to form L-shaped spacers.

2. (CurrentlyAmended) The method of Claim 1, further including ~~the step of~~ forming a liner oxide layer over said gate structure prior to ~~the step of~~ forming the dielectric spacer layer.

3. (Previously Amended) The method of Claim 2 wherein said liner oxide layer is deposited to a thickness of between approximately 20 Angstroms and 200 Angstroms.

4. (Previously Amended) The method of Claim 1 wherein said dielectric spacer layer comprises a nitride layer.

5. (Previously Amended) The method of Claim 3, wherein the said dielectric spacer has a thickness in the range of 150 Angstroms and 500 Angstroms.

6. (Previously Amended) The method of Claim 1 wherein said dielectric spacer layer comprises a silicon oxynitride layer.

7. (Currently Amended) The method of Claim 1 wherein ~~the step of~~ etching said dielectric spacer layer includes anisotropically etching said dielectric spacer layer to form L-shaped spacers, said L-shaped spacers having vertical portions varying in thickness and horizontal portions varying in thickness.

8. (Previously Amended) The method of Claim 7, wherein said and horizontal portion of the L-shaped spacers having bulging profiles varying gradually in thickness from a maximum thickness immediately adjacent the vertical portion of the L-shaped spacer to a portion of the L-shaped spacer furthers from the vertical-portion of the L-shaped spacer, wherein the horizontal portion varies gradually to provide for an average thickness of the L-shaped portion that is 50 to 85 percent of the maximum thickness.

9. (Currently Amended) The method of Claim 7 wherein said dielectric spacer layer is anisotropically etched using a capacitively coupled plasma etch process with an etching chemistry comprising CH3F and O2 in combination with an inert gas to form said L-shaped spacers.

10. (Currently Amended) The method of Claim 7, wherein said dielectric spacer layer is anisotropically etched using an inductively coupled plasma etch process with an etching chemistry comprising CH3F and O2 in combination with an inert gas.

11. (Currently Amended) The method of Claim 1, wherein ~~the step of~~ etching said dielectric spacer layer to form said L-shaped spacers includes using CH3F and O2 chemistry in ratios ranging from approximately 2:1 to approximately 5:1 CH3F to O2.

12. (Currently Amended) The method of Claim 11, wherein ~~the step of~~ etching said dielectric spacer layer to form said L-shaped spacers utilizes a pressure during the etch process ranging from approximately 20 milliTorr to approximately 500 milliTorr.

13. (Currently Amended) The method of Claim 11, wherein ~~the step of~~ etching includes using a temperature ranging from approximately 10 degrees C and 30 degrees C.

14. (Withdrawn) An apparatus comprising a first transistor structure including an L-shaped spacer having a vertical portion varying substantially in thickness over a majority of its length and a horizontal portion varying substantially in thickness over a majority of its length.

15. (Withdrawn) The apparatus of Item 14, wherein said vertical and horizontal portions of L-shaped spacers have a bulging profile which varies gradually in thickness from a maximum thickness immediately adjacent the vertical portion of the L-shaped spacer to a portion of the L-shaped spacer furthest from the vertical-portion of the L-shaped spacer, wherein the horizontal portion varies gradually to provide for an average thickness of the L-shaped portion that is 50 to 85 percent of the maximum thickness.

16. (Withdrawn) The apparatus of Item 14, wherein the length of the horizontal portion of the L-shaped spacer ranges from approximately 80 percent of the deposition thickness to 150 percent of the deposition thickness.

17. (Withdrawn) The apparatus of Item 14 further comprising:

a second transistor immediately adjacent to the first transistor, where in a distance between a sidewall portion of a gate of the first transistor and a sidewall portion of a gate of the second transistor less than 120 nanometers.

18. (Currently Amended) A method for fabricating sidewall spacers in the manufacture of an integrated circuit device, comprising ~~the steps of~~:

providing a substrate having a gate structure formed thereon;

forming a liner oxide layer on said gate structure;

forming a dielectric spacer layer over said liner oxide layer; and

anisotropically etching said dielectric spacer layer without the use of a sacrificial forming layer~~, prior to forming a layer subsequent to the dielectric layer,~~ to form L-shaped spacers, said L-shaped spacers having vertical portions and a horizontal portion, wherein the horizontal portion varies gradually in thickness from a maximum thickness immediately adjacent the vertical portion of the L-shaped spacer to a portion of the L-shaped spacer furthest from the vertical-portion of the L-shaped spacer, wherein the horizontal portion varies gradually to provide for an average thickness of the L-shaped portion that is 50 to 85 percent of the maximum thickness.

19. (New) A method for fabricating sidewall spacers in the manufacture of an integrated circuit device, comprising:

providing a substrate having a gate structure formed thereon;

forming a dielectric spacer layer over the semiconductor substrate having an exposed surface portion adjacent the gate structure; and

etching said exposed surface portion of the dielectric spacer layer to form L-shaped spacers.

20. (New) The method of Claim 19, further including forming a liner oxide layer over said gate structure prior to forming the dielectric spacer layer.

21. (New) The method of Claim 20 wherein said liner oxide layer is deposited to a thickness of between approximately 20 Angstroms and 200 Angstroms.

22. (New) The method of Claim 19 wherein said dielectric spacer layer comprises a nitride layer.

23. (New) The method of Claim 21, wherein the said dielectric spacer has a thickness in the range of 150 Angstroms and 500 Angstroms.

24. (New) The method of Claim 19 wherein said dielectric spacer layer comprises a silicon oxynitride layer.

25. (New) The method of Claim 19 wherein etching said dielectric spacer layer includes anisotropically etching said dielectric spacer layer to form L-shaped spacers, said L-shaped spacers having vertical portions varying in thickness and horizontal portions varying in thickness.

26. (New) The method of Claim 25, wherein said and horizontal portion of the L-shaped spacers having bulging profiles varying gradually in thickness from a maximum thickness immediately adjacent the vertical portion of the L-shaped spacer to a portion of the L-shaped spacer furthers from the vertical-portion of the L-shaped spacer, wherein the horizontal portion

varies gradually to provide for an average thickness of the L-shaped portion that is 50 to 85 percent of the maximum thickness.

27. (New) The method of Claim 25 wherein said dielectric spacer layer is anisotropically etched using a capacitively coupled plasma etch process with an etching chemistry comprising CH3F and O2 in combination with an inert gas to form said L-shaped spacers.

28. (New) The method of Claim 25, wherein said dielectric spacer layer is anisotropically etched using an inductively coupled plasma etch process with an etching chemistry comprising CH3F and O2 in combination with an inert gas.

29. (New) The method of Claim 19, wherein etching said dielectric spacer layer to form said L-shaped spacers includes using CH3F and O2 chemistry in ratios ranging from approximately 2:1 to approximately 5:1 CH3F to O2.

30. (New) The method of Claim 29, wherein etching said dielectric spacer layer to form said L-shaped spacers utilizes a pressure during the etch process ranging from approximately 20 milliTorr to approximately 500 milliTorr.

31. (New) The method of Claim 29, wherein etching includes using a temperature ranging from approximately 10 degrees C and 30 degrees C.

32. (New) A method for fabricating sidewall spacers in the manufacture of an integrated circuit device, comprising:

providing a substrate having a gate structure formed thereon;

forming a dielectric spacer layer over the semiconductor substrate; and

etching said dielectric spacer layer, prior to forming any layer overlying the dielectric layer, to form L-shaped spacers.